IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	10/068,492	Confirmation No.: 7292
Appellant:	Tsecouras	
Filed:	02/05/2002	
TC/AU:	2617	
Examiner:	Bhattacharya	
Docket:	TI-33116	
Cust.No.:	23494	

APPELLANT'S BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

The attached sheets contain the Rule 41.37 items of appellant's brief; this brief is pursuant to MPEP 1204.01 (Reinstatement of Appeal). The fee for filing a brief in support of the appeal has previously been paid; but the Commissioner is hereby authorized to charge any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Claims 1-29 are pending in the application with all claims finally rejected. This appeal involves the finally rejected claims.

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The apparatus of claims 1, 12, and 18 and the method of claim 25 all relate to frequency control in a digital amplifier in conjunction with a sample rate converter to change the sample rate of incoming digital signals. Application Fig. 2 item 202 is the sample rate converter, and page 4, second paragraph notes that this allows changing the digital amplifier switching frequency to avoid generation of interference in (selectable) frequency bands.

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

(1) Claims 1-5, 11-15, 18-21, 24-25, and 28-29 were rejected as unpatentable over the Matsushita reference in view of the Orndorff and Groshong references.

(2) Claims 6-10, 16-17, 22-23, and 26-27 were rejected as unpatentable over the Matsushita reference in view of the Orndorff, Groshong, and Midya references.

Rule 41.37(c)(1)(vii) Arguments

(1) Claims 1-5, 11-15, 18-21, 24-25, and 28-29 were rejected as unpatentable over Matsushita in view of Orndorff and Groshong.

With regard to claim 1, the Examiner pointed to Matsushita Fig.7, item 74 (col.6, ln.40-43) as the sample rate converter required by claim 1.

Appellant replies that Matsushita Fig.7, item 74 (col.6, ln.40-43) is an analog-to-digital converter which converts an analog input signal to digital output samples at some sample rate. In contrast, a sample rate converter as in claim 1 converts input digital samples at a first sample rate into output digital samples at a second sample rate. Thus Matsushita has no suggestion of claim 1, and Orndorff and Groshong (which were added to show control data bits and user selection) add nothing suggesting a sample rate converter. Consequently, claim 1 is patentable over the references.

With regard to claim 12, the Examiner again points to Matsushita Fig.7, item 74 (col.6, ln.40-43) for the sample rate converter required by claim 12.

Appellant repeats the foregoing argument that Matsushita Fig.7, item 74 (col.6, ln.40-43) is an analog-to-digital converter, not a sample rate converter and that, consequently, claim 12 is patentable over the references.

With regard to claim 18, the Examiner refers to the rejection of claim 12.

Appellant also refers to the argument for claim 12, that Matsushita Fig.7, item 74 (col.6, ln.40-43) is an analog-to-digital converter and does not suggest a sample rate converter as required by claim 12.

With regard to method claim 25, the Examiner again points to Matsushita col.6, ln.40-43 for the sample rate converter required by the claim.

Appellant repeats the argument that Matsushita col.6, ln.40-43 describe an analog-to-digital converter, not the required sample rate converter and that, consequently, claim 25 is patentable over the references.

For the dependent claims, appellant relies upon the patentability of the parent claims (claims 1, 12, 18, and 25).

(2) Claims 6-10, 16-17, 22-23, and 26-27 were rejected as unpatentable over Matsushita in view of Orndorff, Groshong, and Midya.

Appellant relies upon the patentability of parent claims 1, 12, 18, and 25.

Rule 41.37(c)(1)(viii) Claims appendix

1. A digital amplifier adaptive pulse frame rate frequency control system comprising:

a sample rate converter;

a programmable controller operational in response to user selected input frequency data to generate control data bits; and

a system clock generator operational to generate a sample rate converter master clock signal in response to the control data bits such that the sample rate converter generates output data at a sample rate determined by the control data bits.

2. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a digital signal processor (DSP), a CPU, and a micro-controller.

3. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

4. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the system clock generator is further operational to generate audio clock signals at the sample rate determined by the control data bits.

5. The digital amplifier adaptive pulse frame rate frequency control system according to claim 4 wherein the system clock generator is further operational to generate sample clock signals at the sample rate determined by the control data bits.

6. The digital amplifier adaptive pulse frame rate frequency control system according to claim 4 further comprising a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data.

7. The digital amplifier adaptive pulse frame rate frequency control system according to claim 6 wherein the digital amplifier output further switches at a pulse-frame rate to minimize interference associated with keep-out bands for frequencies related to a desired source.

8. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of AM, FM and TV band frequencies.

9. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of radio frequency (RF), intermediate frequency (IF), and Local Control Oscillator (LCO) frequencies.

10. The digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with wireless communication frequencies selected from the group consisting of cellular telephone frequencies and Bluetooth frequencies.

11. The digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the sample rate converter comprises a digital asynchronous sample rate converter.

12. A digital amplifier adaptive pulse frame rate frequency control system comprising:

a digital asynchronous sample rate converter operational to generate output audio data in response to input audio data, an input audio clock and a master clock;

a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies;

a decoder operational to decode the control data bits; and

a system clock generator operational to generate the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converter generates the output data at a sample rate determined by the user selected input frequency information.

13. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a DSP, a CPU, and a micro-controller.

14. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

15. The digital amplifier adaptive pulse frame rate frequency control system according to claim 12 wherein the system clock generator is further operational to generate audio clocks at the sample rate determined by the user selected input frequency information.

16. The digital amplifier adaptive pulse frame rate frequency control system according to claim 15 further comprising a digital amplifier responsive to the system clock generator audio clocks and the digital asynchronous sample rate converter output audio data such that the digital amplifier output switches at a pulse-frame rate determined by the user selected input frequency information.

17. The digital amplifier adaptive pulse frame rate frequency control system according to claim 16 wherein the digital amplifier output switches at a pulse-frame rate to minimize interference with keep-out bands associated with the input frequency information.

18. A digital amplifier adaptive pulse frame rate frequency control system comprising:

digital asynchronous sample rate converting means for generating output audio data in response to input audio data, an input audio clock and a master clock;

programmable controlling means for generating control data bits in response to user selected input frequency information, wherein the input frequency information is selected from the group consisting of RF, IF, LCO, AM, FM, TV, wireless, cellular telephone and Bluetooth band frequencies;

decoding means for decoding the control data bits; and

clock generating means for generating the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converting means generates the output data at a sample rate determined by the user selected input frequency information.

19. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the programmable controlling means comprises a data processing device selected from the group consisting of a computer, a DSP, a CPU, and a micro-controller.

20. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop.

21. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means is further operational to generate audio clocks at the sample rate determined by the user selected input frequency information.

22. The digital amplifier adaptive pulse frame rate frequency control system according to claim 21 further comprising a digital amplifying means for generating an output signal that switches at a pulse-frame rate determined by the user selected input frequency information in response to the clock generating means audio clocks and the digital asynchronous sample rate converting means output audio data.

23. The digital amplifier adaptive pulse frame rate frequency control system according to claim 22 wherein the digital amplifying means output signal further switches at a pulse-frame rate that minimizes interference with keep-out bands associated with input frequency information.

24. The digital amplifier adaptive pulse frame rate frequency control system according to claim 18 wherein the clock generating means is further operational to generate sample clocks at the sample rate determined by the user selected input frequency information.

25. A method of controlling the pulse-frame rates for a digital amplifier output signal comprising the steps of:

providing a pulse-frame rate frequency control system having a programmable controller, a system clock generator, and a digital asynchronous sample rate

converter operational to generate output audio data at a first sample rate in response to input audio data and further in response to input audio clocks;

communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data;

communicating the control data bits to the system clock such that the system clock generates a master clock for the digital asynchronous sample rate converter at a new sample rate and further such that the system clock generates output audio clocks at the new sample rate; and

adapting the digital asynchronous sample rate converter output audio data at a first sample rate to conform to the new sample rate determined by the master clock.

26. The method according to claim 25 further comprising the steps of:

providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and

communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate.

27. The method according to claim 25 further comprising the steps of:

providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and

communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate to a new pulse-frame rate that substantially minimizes interference

minimizes interference with keep-out bands associated with the frequency group consisting of AM, FM, and TV band frequencies.

28. The method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing a look-up table of pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits.

29. The method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing an algorithm to select pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none